

FIG. 1

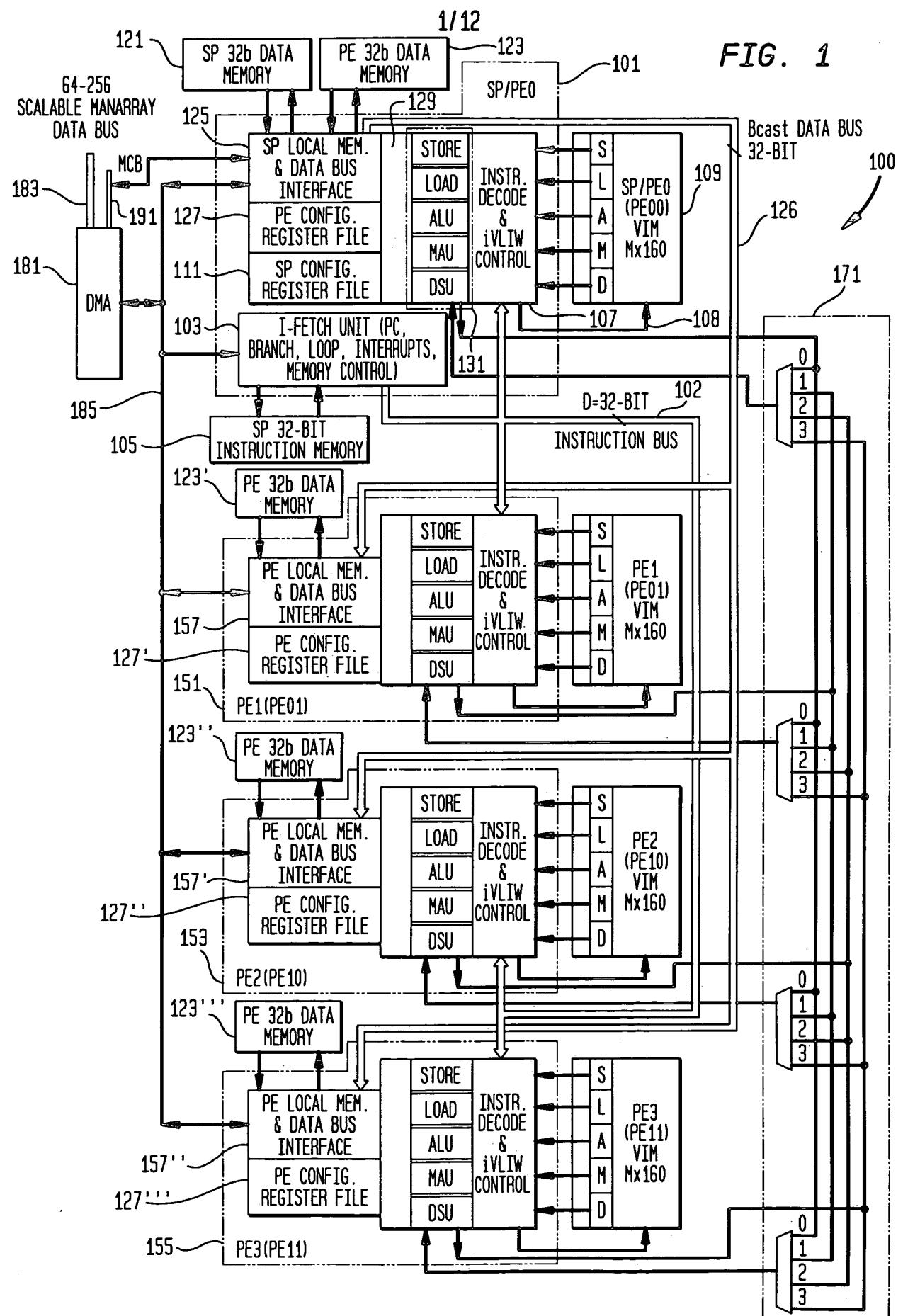


FIG. 2A

196	MCB ADDRESS: 0x0070030																SPR ADDRESS: 0x0030																RESET VALUE: 0x00000000																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																
INTONLY	ANY VALUE																SleepCNT																																														

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FIG. 2B

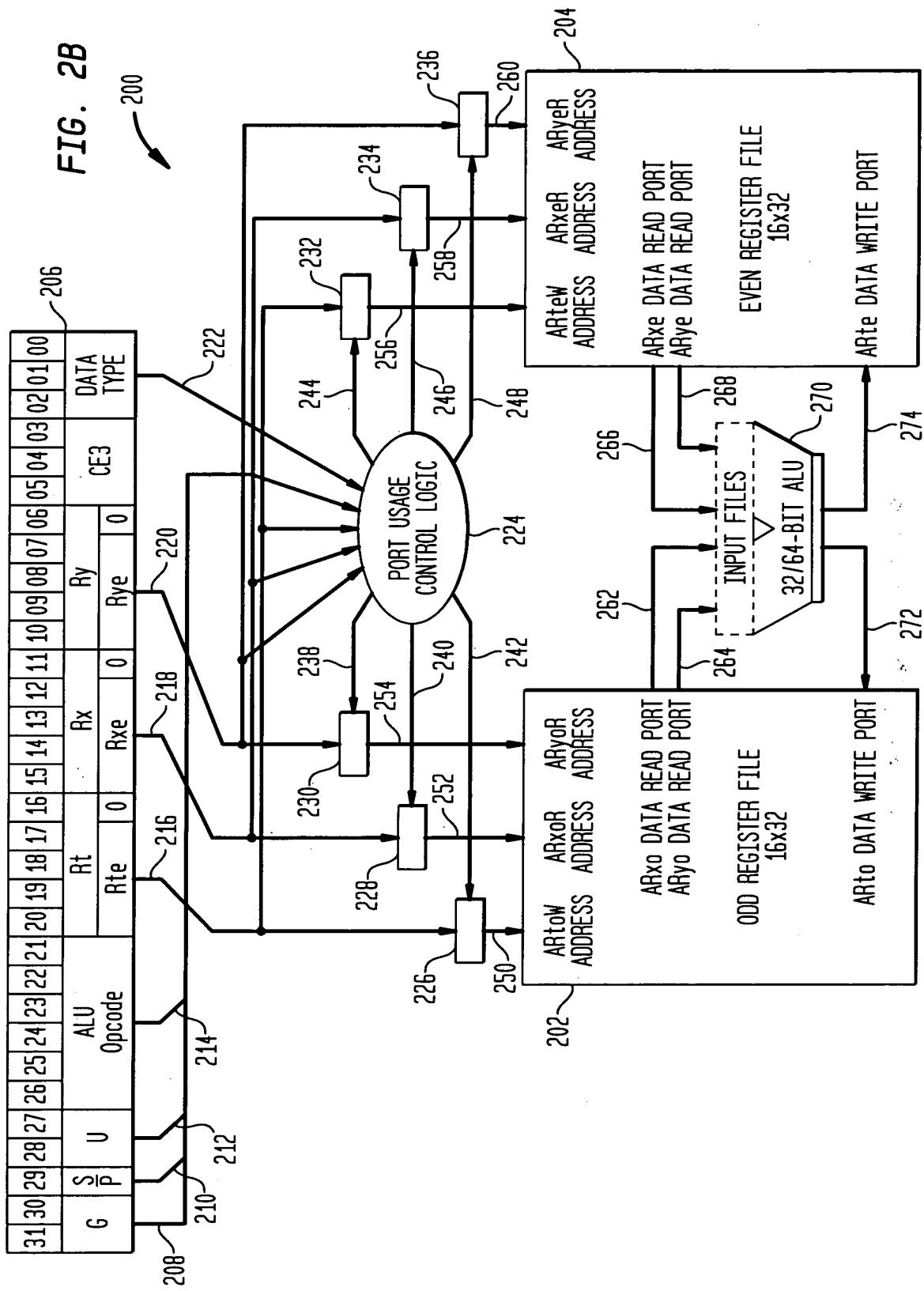


FIG. 3A

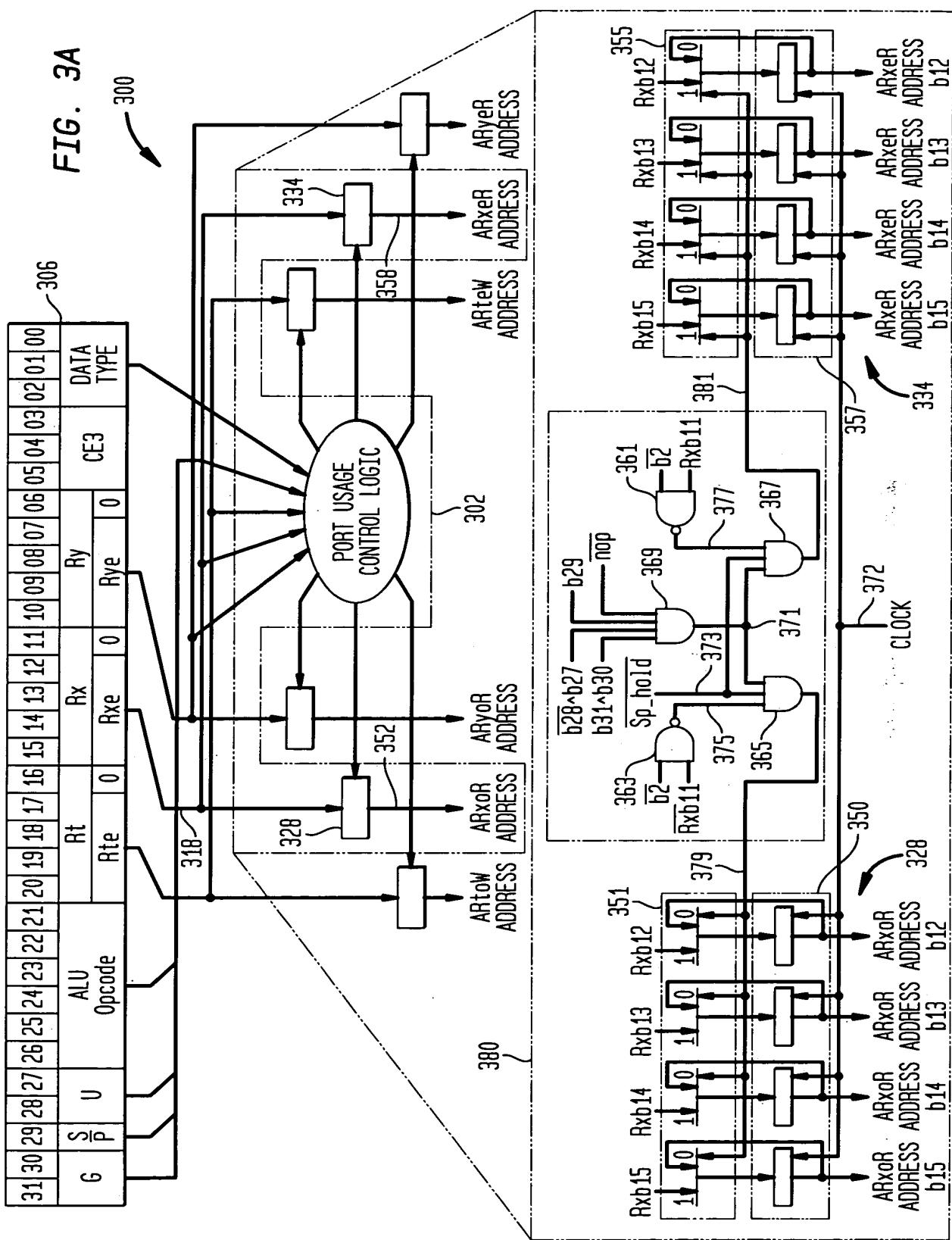
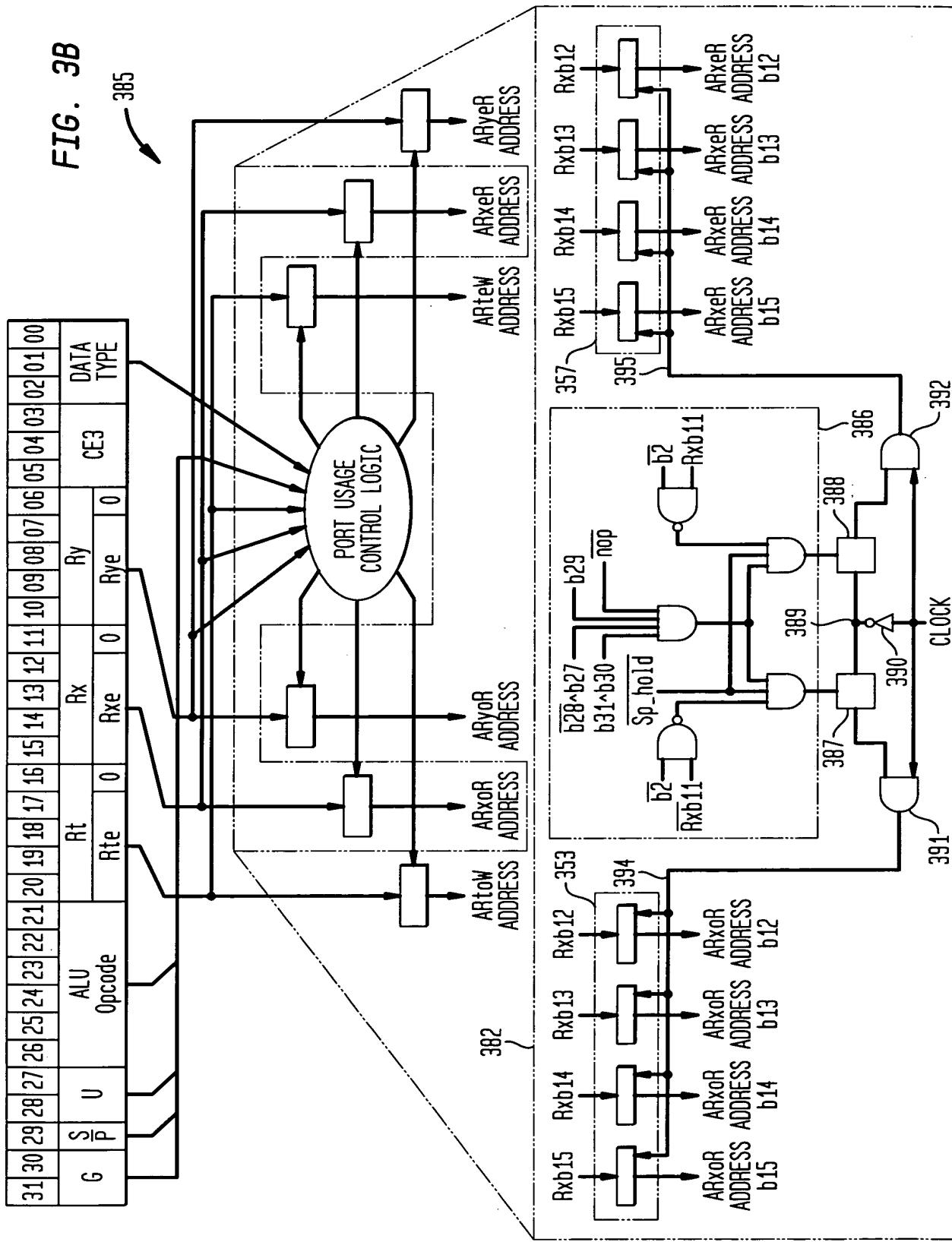
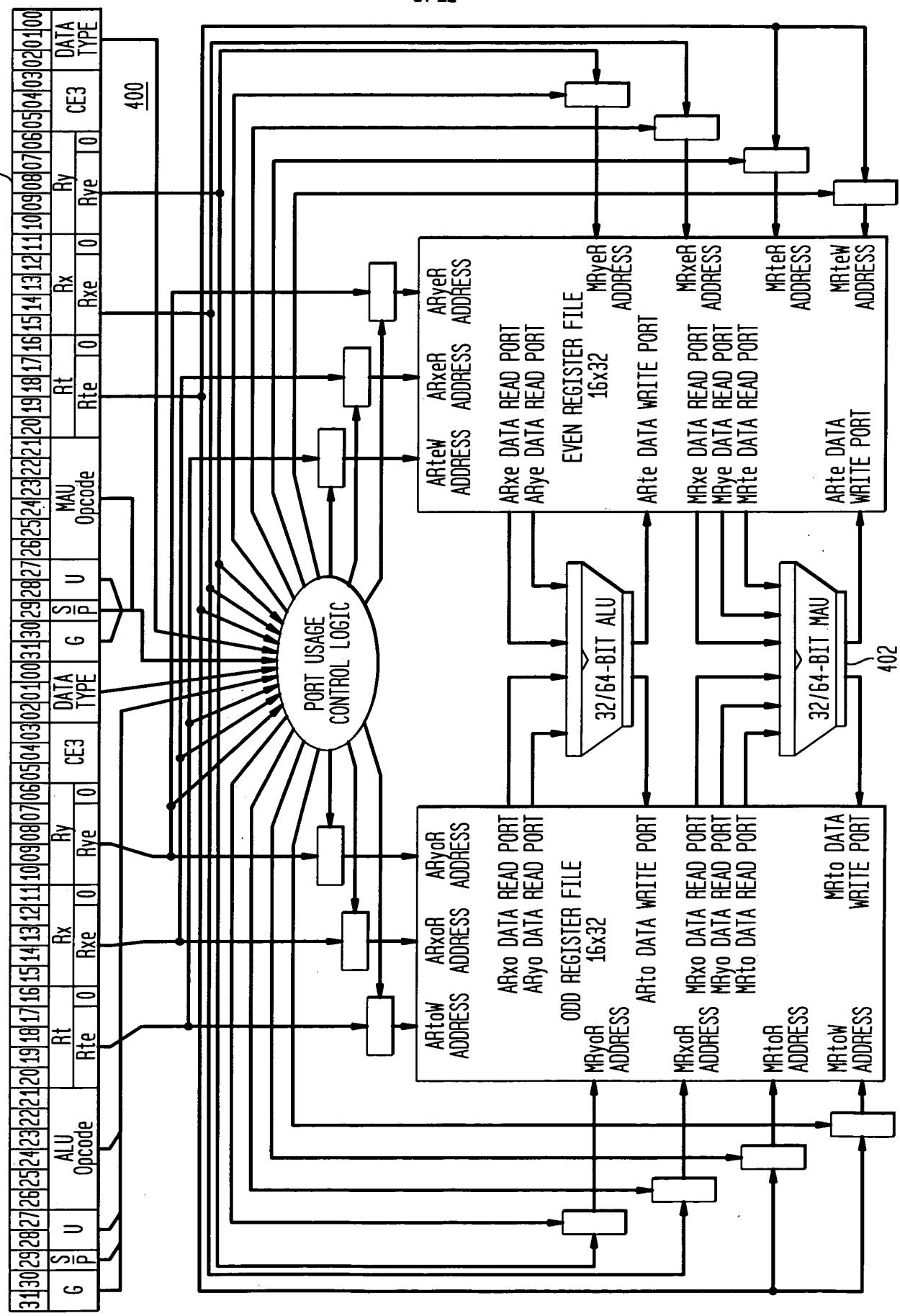


FIG. 3B

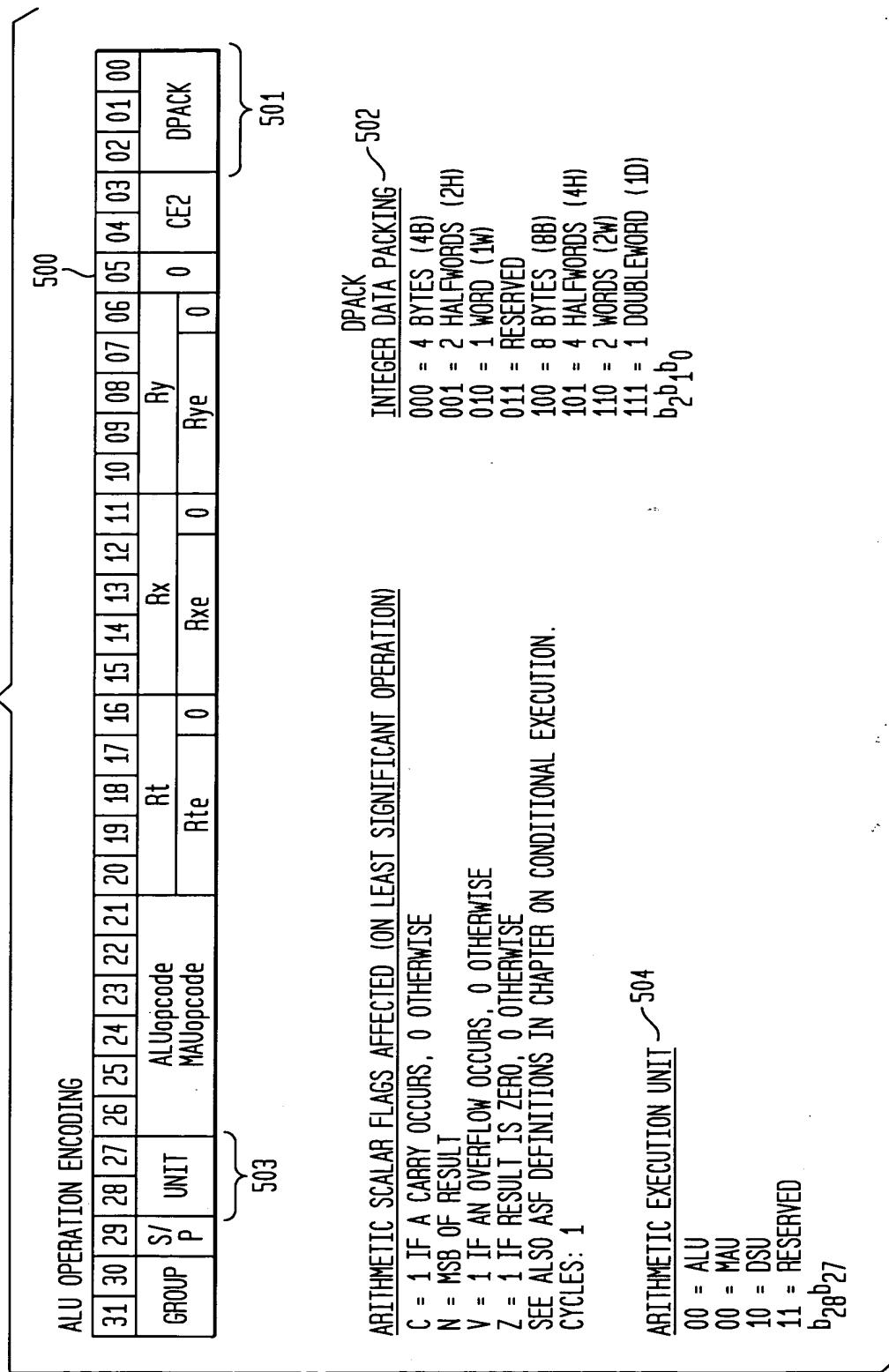


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FIG. 5A



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FIG. 5B

DESCRIPTION

THE SUM OF SOURCE REGISTERS Rx AND Ry IS STORED IN TARGET REGISTER Rt.
SYNTAX/OPERATION

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INSTRUCTION	OPERANDS	OPERATION	ACF
DOUBLEWORD			
ADD.[SP][AM].1D	Rte, Rxe, Rye	Rt ₀ Rte \leftarrow Rx ₀ Rx _e + Ry _e Rye	NONE
[TF].ADD.[SP][AM].1D	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
WORD			
ADD.[SP][AM].1W	Rt, Rx, Ry	Rt \leftarrow Rx + Ry	NONE
[TF].ADD.[SP][AM].1W	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
DUAL WORDS			
ADD.[SP][AM].2W	Rte, Rxe, Rye	Rt ₀ \leftarrow Rx ₀ + Ry ₀ Rt _e \leftarrow Rx _e + Ry _e	NONE
[TF].ADD.[SP][AM].2W	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
DUAL HALFWORDS			
ADD.[SP][AM].2H	Rt, Rx, Ry	Rt.H1 \leftarrow Rx.H1 + Ry.H1 Rt.H0 \leftarrow Rx.H0 + Ry.H0	NONE
[TF].ADD.[SP][AM].2H	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
QUAD HALFWORDS			
ADD.[SP][AM].4H	Rte, Rxe, Rye	Rt ₀ .H1 \leftarrow Rx ₀ .H1 + Ry ₀ .H1 Rt ₀ .H0 \leftarrow Rx ₀ .H0 + Ry ₀ .H0 Rt _e .H1 \leftarrow Rx _e .H1 + Ry _e .H1 Rt _e .H0 \leftarrow Rx _e .H0 + Ry _e .H0	NONE
[TF].ADD.[SP][AM].4H	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
QUAD BYTES			
ADD.[SP][AM].4B	Rt, Rx, Ry	Rt.B3 \leftarrow Rx.B3 + Ry.B3 Rt.B2 \leftarrow Rx.B2 + Ry.B2 Rt.B1 \leftarrow Rx.B1 + Ry.B1 Rt.B0 \leftarrow Rx.B0 + Ry.B0	NONE
[TF].ADD.[SP][AM].4B	Rt, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE
OCTAL BYTES			
ADD.[SP][AM].8B	Rte, Rxe, Rye	Rt ₀ .B3 \leftarrow Rx ₀ .B3 + Ry ₀ .B3 Rt ₀ .B2 \leftarrow Rx ₀ .B2 + Ry ₀ .B2 Rt ₀ .B1 \leftarrow Rx ₀ .B1 + Ry ₀ .B1 Rt ₀ .B0 \leftarrow Rx ₀ .B0 + Ry ₀ .B0 Rt _e .B3 \leftarrow Rx _e .B3 + Ry _e .B3 Rt _e .B2 \leftarrow Rx _e .B2 + Ry _e .B2 Rt _e .B1 \leftarrow Rx _e .B1 + Ry _e .B1 Rt _e .B0 \leftarrow Rx _e .B0 + Ry _e .B0	NONE
[TF].ADD.[SP][AM].8B	Rte, Rxe, Rye	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE

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MPYA-MULTIPLY ACCUMULATE
ENCODING

FIG. 6A

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GROUP	S/P	UNIT	MAUopcode		Rte	0	Rx	Ry		CE3	MPACK																				

SYNTAX/OPERATION

FIG. 6B

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INSTRUCTION	OPERANDS	OPERATION	ACF WORD
MPYA.[SP]M.1[SU]W	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA[CNVZ].[SP]M.1[SU]W	Rte, Rx, Ry	Rto Rte \leftarrow Rto Rte + (Rx * Ry)	F0
[TF].MPYA.[SP]M.1[SU]W	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN ACFs	NONE
DUAL HALFWORDS			
MPYA.[SP]M.2[SU]H	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA[CNVZ].[SP]M.2[SU]H	Rte, Rx, Ry	Rto \leftarrow Rto + (Rx.H1 * Ry.H1) Rte \leftarrow Rte + (Rx.H0 * Ry.H0)	F1 F0
[TF].MPYA.[SP]M.2[SU]H	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN ACFs	NONE
QUAD BYTES			
MPYA.[SP]M.4[SU]B	Rte, Rx, Ry	DO OPERATION BELOW BUT DO NOT AFFECT ACFs	NONE
MPYA[CNVZ].[SP]M.4[SU]B	Rte, Rx, Ry	Rto.H1 \leftarrow Rto.H1 + (Rx.B3 * Ry.B3) Rto.H0 \leftarrow Rto.H0 + (Rx.B2 * Ry.B2) Rte.H1 \leftarrow Rte.H1 + (Rx.B1 * Ry.B1) Rte.H0 \leftarrow Rte.H0 + (Rx.B0 * Ry.B0)	F3 F2 F1 F0
[TF].MPYA.[SP]M.4[SU]B	Rte, Rx, Ry	DO OPERATION ONLY IF T/F CONDITION IS SATISFIED IN F0	NONE

FIG. 6C

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ARITHMETIC SCALAR FLAGS AFFECTED
(ON LEAST SIGNIFICANT OPERATION)

C = NOT AFFECTED
 N = MSB OF RESULT
 V = NOT AFFECTED
 Z = 1 IF RESULT IS ZERO,
 0 OTHERWISE
 CYCLES: 2

ARITHMETIC EXECUTION UNIT

00 = ALU
 00 = MAU
 10 = DSU
 11 = RESERVED
 $b_{28}b_{27}$

INSTRUCTION GROUP

00 = RESERVED
 00 = FLOW CONTROL
 10 = LOAD/STORE (LU, SU)
 11 = ARITHMETIC/LOGICAL
 (ALU, MAU, DSU)
 $b_{31}b_{30}$

MPACK-MULTIPLY DATA PACKING

000 = RESERVED
 001 = 2 HALFWORDS (2H)
 010 = 1 WORD (1W)
 011 = RESERVED
 100 = RESERVED
 101 = 4 HALFWORDS (4H)
 FOR MPYH AND MPYL
 110 = RESERVED
 111 = RESERVED
 $b_2b_1b_0$
SP/PE SELECT
 0 = SP
 1 = PE

FIG. 7A

RECEIVED 32-BIT XV INSTRUCTION

ENABLE MASK BITS

31 30	29 28	25 24	23 22	21 20	19 18	17	10 9	8 7	6
Group S/P	XV opcode	Vx	UAF	RFI	0 0	0 0	S L A M D	Vb 0	VIMOFFS

IR1

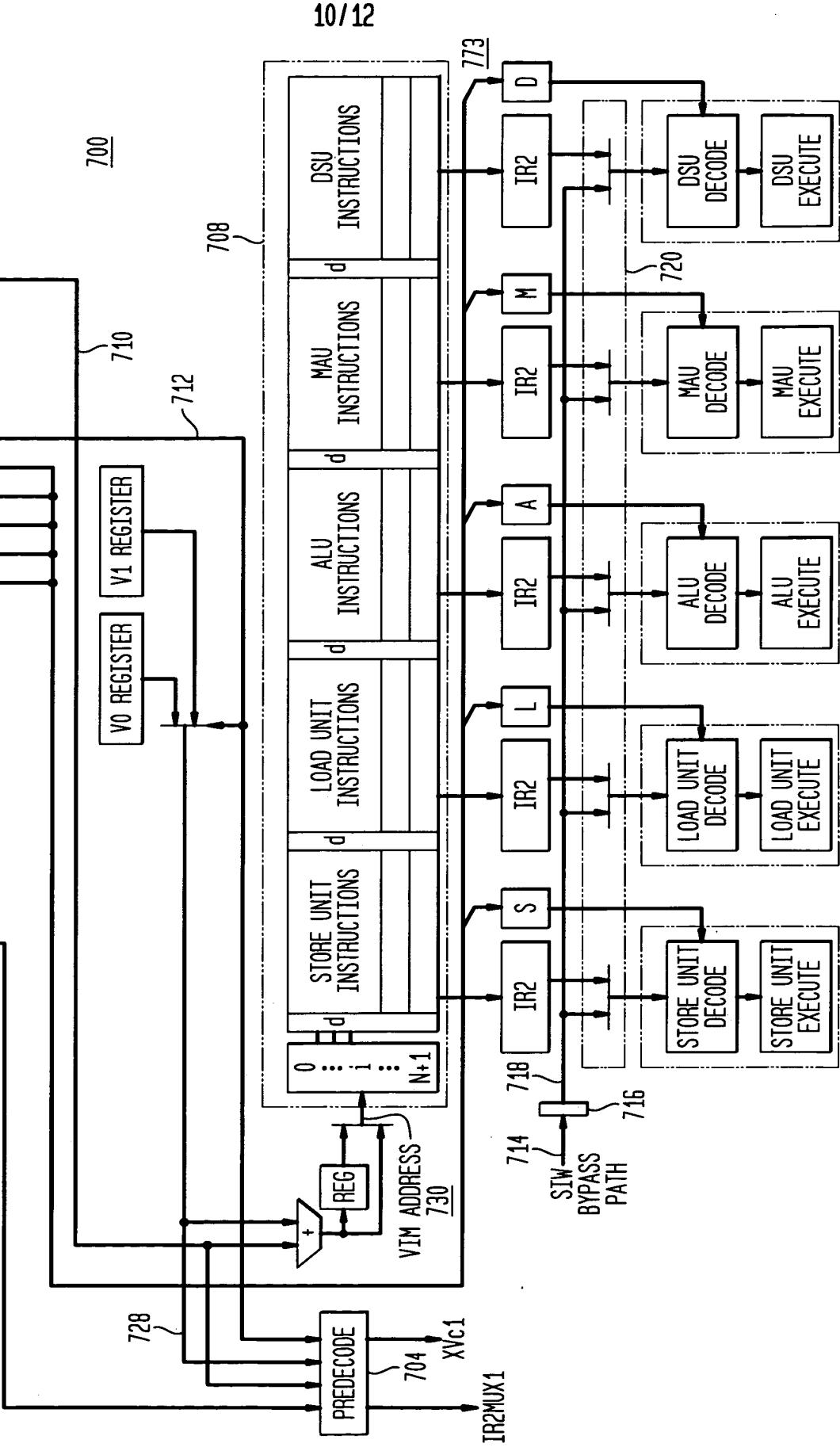
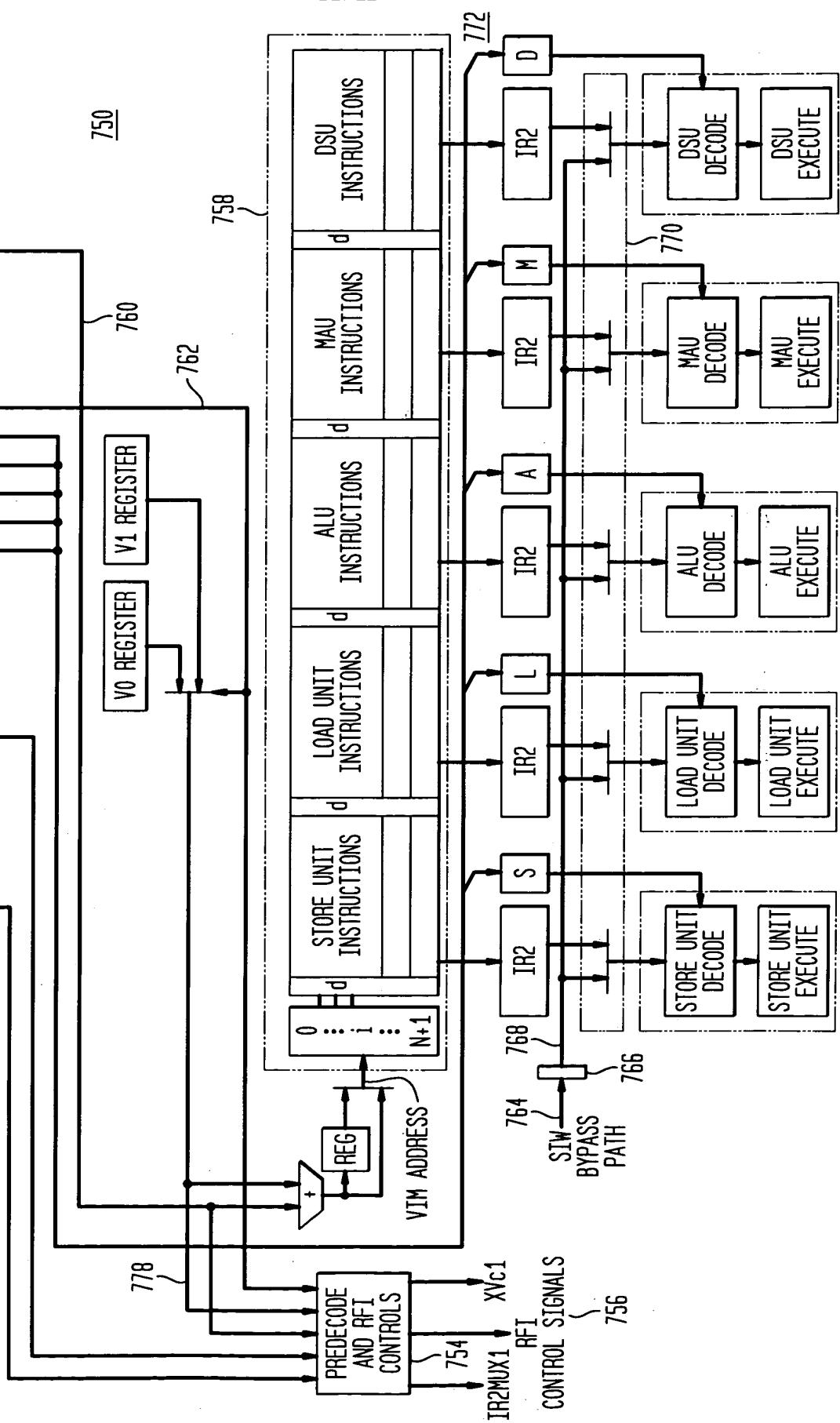
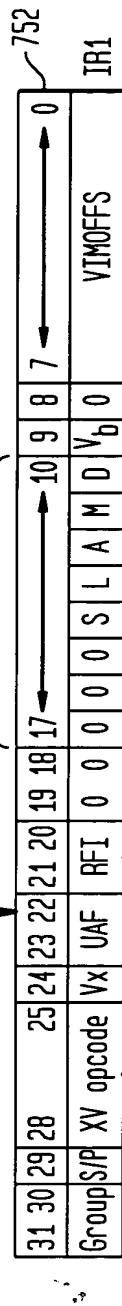


FIG. 7B

RECEIVED 32-BIT XV INSTRUCTION

ENABLE MASK BITS



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FIG. 8

